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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/696,079

10/29/2003

Sangwoo Lim

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EXAMINER

MAI, ANH D

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/696,079

Applicant(s)

LIM ET AL.

Examiner

Anh D. Mai

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 February 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) 25-28 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 October 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/30/2003</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of invention Group I, claims 1-24 in the reply filed on February 22, 2005 is acknowledged. The traversal is on the ground(s) that the method (process) and the integrated circuit (apparatus) are not distinct invention. This is not found persuasive because Applicant fails to provide any evidence to the contrary that the claimed device can be made by other method.

The requirement is still deemed proper and is therefore made **FINAL**.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested:

METHOD FOR FORMING DUAL GATE OXIDE THICKNESS UTILIZING ASHING
AND CLEANING.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the **SOI substrate** (as recites in claim 2) and **the triple gate oxide** (TGO) process (as recites in claim 23) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Art Unit: 2814

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, line 15, recites: "**ashing** the portion of remaining dielectric layer within the region...".

Art Unit: 2814

It is well known in the art that "ashing" is a plasma process to remove the photoresist material. Ashing does not affect the dielectric layer but it may oxidize the substrate, hence increasing the thickness of the existing dielectric layer. (See instant page 7, lines 18-20).

Thus, **ashing** the dielectric layer is indefinite in this context.

For more information about **ashing**, see U.S. Patent No. 5,086,017 and 5,190,887.

Claim 4 recites: "wherein the region includes a high performance device region.

What is the *high performance device* ?

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-14 and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek et al. (U.S. Pub. No. 2003/0157772) in view of Vogel et al. (U.S. Patent No. 5,631,178).

With respect to claim 1, as best understood by the examiner, Wieczorek teaches a method for forming a multigate dielectric structure for a semiconductor device substantially as claimed including:

providing a substrate (1), the substrate having a surface with a first surface roughness;

Art Unit: 2814

providing a dielectric layer (5) overlying the substrate (1) and forming a dielectric/substrate interface between the dielectric layer (5) and the substrate (1) at the surface of the substrate, the dielectric layer (5) having an initial thickness;

forming a patterned photoresist (6) overlying the dielectric layer (5) and the substrate, the patterned photoresist (5) defining a region (3) for formation of a gate dielectric of a desired target thickness;

etching the region (3) so that a portion of the dielectric layer (7') remains within the region (3), wherein the portion of remaining dielectric layer (7') within the region (3) has a first intermediate thickness, the first intermediate thickness being less than the initial thickness;

removing the photoresist following the thinning of the dielectric layer; and

thermally oxidizing the dielectric layer (7'), wherein thermally oxidizing causes the portion of remaining dielectric layer (7') within the region (3) to have a desired target thickness, and further wherein the thermal oxidation increases a density of the portion of remaining dielectric layer. (See Figs. 4).

Thus, Wieczorek is shown to teach all the features of the claim with the exception of detailing the removal of the photoresist layer.

However, Vogel teaches the process to remove a photoresist is well known in the art including: plasma oxygen ashing process followed by piranha clean. (See col. 3, lines 25-38).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the photoresist of Wieczorek by plasma oxygen ashing and wet cleans as taught by Vogel, since the process are well known in the art.

The plasma ashing inherently exposes the dielectric layer (7') to oxygen plasma thus causes an increase in thickness of the dielectric layer remaining within the region (3) from the first intermediate thickness to a second intermediate thickness; and the wet clean inherently causes a decrease in thickness of the dielectric layer remaining within the region (3) from the second intermediate thickness to a third intermediate thickness.

With respect to claim 2, the substrate of Wieczorek includes a bulk substrate.

With respect to claim 3, the dielectric layer of Wieczorek includes a silicon dioxide layer.

With respect to claim 4, the region of Wieczorek includes a high performance device region.

With respect to claim 5, the portion of the dielectric layer remaining within the region (3) of Wieczorek further prevents the dielectric/substrate interface from subsequently being breached by the etchant.

With respect to claim 6, the first intermediate thickness (7') of Wieczorek is reduced from the initial thickness.

Thus, Wieczorek is shown to teach all the features of the claim with the exception of explicitly disclosing the thickness to be less than 10 Å. Note that the claimed thickness does not appear to be critical.

However, Wieczorek teaches a very thin oxide layers, within the range of some tenths of a nanometer (nm) can be formed. (See [0057]).

Note that the specification contains no disclosure of either the *critical nature of the claimed thickness of 10 Å* of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the dielectric layer of the first intermediate thickness of Wieczorek without exposing the substrate since the removal rate of the etchant is known and it is within the ability of the skill worker in the art to form the dielectric layer without exposing the substrate.

With respect to claim 7, ashing of Wieczorek, in view of Vogel further includes ashing the patterned photoresist for removing the patterned photoresist.

With respect to claim 8, the second intermediate thickness (some tenths of a nanometer) of Wieczorek includes the claimed range (18 Å). Note that the claimed thickness does not appear to be critical.

Note that the specification contains no disclosure of either the *critical nature of the claimed thickness of 10 Å* of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Art Unit: 2814

With respect to claim 9, ashing of Wieczorek, in view of Vogel, includes exposing the portion of remaining dielectric layer (7') to an oxygen plasma.

With respect to claim 10, the method of Wieczorek, in view of Vogel, further comprises subsequent to ashing, performing a post-ashing clean.

With respect to claim 11, the post-ashing clean as taught by Vogel includes use of a sulfuric acid peroxide mixture (SPM).

With respect to claim 12, cleaning as taught by Vogel, includes a preclean.

With respect to claims 13 and 14, a duration of the preclean of Wieczorek, in view of Vogel is selected such that the preclean does not affect the first surface roughness of the substrate layer within the region.

Since the dielectric layer (7') remain on the region (3), the surface roughness of the substrate is protected, thus, the limitation is met.

With respect to claim 18, in view of Vogel, the cleaning process inherently reduces the thickness of the dielectric layer remaining within the region from the second intermediate thickness to a third intermediate thickness. Since the cleaning solution only remove a small thickness of the dielectric layer, therefore, the thickness of the third intermediate is obviously fall within the intended thickness (some tenths of nanometer) of Wieczorek.

Note that the claimed thickness does not appear to be critical.

Note that the specification contains no disclosure of either the *critical nature of the claimed thickness of 10 Å* of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the

Art Unit: 2814

Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claim 19, the dielectric layer of Wieczorek, in view of Vogel, includes a first thermal oxide, and wherein thermal oxidation of the dielectric layer forms a second thermal oxide at the dielectric/substrate interface, wherein the portion of the dielectric layer remaining within the region includes a composite of the first thermal oxide, a plasma oxide, and the second thermal oxide, and wherein thermal oxidation further densifies the first thermal oxide and the plasma oxide of the composite remaining within the region.

With respect to claim 20, the method of Wieczorek further includes the surface roughness of the dielectric/substrate interface is substantially preserved.

With respect to claim 21, the method of Wieczorek, in view of Vogel, substantially preserved dielectric/substrate surface roughness is a resultant surface roughness of the dielectric/substrate interface within the region that is substantially similar to the initial surface roughness of the dielectric/substrate interface.

With respect to claim 22, the portion of remaining dielectric layer (7') of Wieczorek is devoid of chemical oxide incorporation at the dielectric/substrate interface.

With respect to claim 23, the method of Wieczorek includes one of a dual gate oxide (DGO) process.

With respect to claim 24, the method of Wieczorek further comprises forming a semiconductor device structure (10) using a portion of the portion of remaining dielectric layer

Art Unit: 2814

within the region as a gate dielectric and forming another semiconductor device structure using a portion of the dielectric layer outside the region as a gate dielectric. (See Fig. 6).

6. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek '772 and Vogel '178 as applied to claim 12 above, and further in view of Schulz (U.S. Patent No. 5,637,151).

With respect to claim 15, Wieczorek and Vogel are shown to teach all the features of the claim with the exception of the preclean further includes a hydrochloric acid peroxide mixture (HPM) clean.

However, Schulz teaches a well known cleaning process includes: a piranha clean, followed by an ammonium peroxide mixture (APM) clean (SC1) and a hydrochloric acid peroxide mixture (HPM) clean (SC2). (See Fig. 1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to perform the preclean of Wieczorek and Vogel to include a hydrochloric acid peroxide mixture (HPM) clean (SC2) as taught by Schulz reduce the metal concentration remaining on the substrate after cleaning sequences.

With respect to claim 16, the APM clean of Wieczorek and Vogel, in view of Schulz is of a limited time duration, the limited time duration being determined as a function of a beginning thickness and a desired target ending thickness.

With respect to claim 17, the piranha clean of Wieczorek in view of Vogel and Schulz includes use of a sulfuric acid peroxide mixture (SPM).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**ANH D. MAI
PRIMARY EXAMINER**

March 17, 2005